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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
MAIS, MARK A	

ART UNIT	PAPER NUMBER
2664	8

DATE MAILED: 08/25/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/736,947	Applicant(s) ZAUN ET AL.	
	Examiner Mark A Mais	Art Unit 2664	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-25 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-25 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 14 December 2000 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date papers 5-7.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Priority

1. Acknowledgement is made of the claim for priority under 35 U.S.C. 120 (Provisional Application 60/170,531 filed on December 14, 1999).

Information Disclosure Statement

2. The information disclosure statements (IDSs) submitted on 13 April 2001, 22 January 2002, and 13 June 2002, were filed after the mailing date of the Application on 14 December 2000. The submission is in compliance with the provisions of 37 CFR 1.56 and 1.97. Accordingly, the examiner considered the information disclosure statements.

Claim Objections

3. Claim 15 is objected to because of the following informalities: It contains a previously undefined reference to "MPS". Appropriate correction is required.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

5. Claims 1-25 are rejected under 35 U.S.C. 102(e) as being anticipated by Robinett et al. (USP 6,351, 471).

6. With regard to claims 1-2, and 12, Robinett et al. discloses a re-multiplexer module **(Figs. 1 and 2, remultiplexers 30 and 100; col. 13, lines 39-41)** for transmitting a plurality of output data streams **(Fig. 2, transport streams (TSs) TS4 and TS5; col. 12, lines 59-62)** from a plurality of input data streams **(Fig. 2, TS1, TS2, and TS3; col. 12, lines 58-59)**, comprising:

an input processing portion with a plurality of processors **(Fig. 2, interpreted as the combination of data link control 112 and direct memory access (DMA) control 116 within interface 110; col. 14, lines 23-32)** that receives a plurality of input data streams **(Fig. 2, TS1, TS2, and TS3; col. 12, lines 58-59)** containing data packets **(col. 6, lines 8-14)** through a plurality of interfaces to be sent to one of the plurality of processors **(Fig. 2, each adapter 110 receives one input stream and it is necessarily inherent that the TS would be input through an interface in order to reach data link controller 112 and DMA controller 116)**;

a plurality of packet buffers for storing data packets of said input streams **(Fig. 2, each**

one of multiple adapters 110 (col. 13, lines 55-56) contains a transport packet cache 114 for storing transport packets from one TS (col. 14, lines 47-54) which is then mapped to a corresponding memory location 122 within host memory 120 by DMA controller 116, col. 18, lines 45-67);

an output processing portion **(Fig. 2, interpreted as the combination of data link control 112 and direct memory access (DMA) control 116 within each one of several interfaces 110; col. 14, lines 23-32)** that selectively multiplexes data packets from said plurality of buffers **(col. 12, line 58 to col. 13, line 7)** to generate at least two output data streams **(Fig. 2, transport streams (TSs) TS4 and TS5; col. 12, lines 59-62)** for outputting the output stream through an interface **(Fig. 2, each adapter 110 receives one output stream and it is necessarily inherent that each TS would be output through one interface in order to reach its intended audience)**; and

a host processor that controls the operation of the input processing portion and the output processing portion **(Fig. 2, controller 160; col. 13, lines 59-65; *see also* col. 10, lines 45-59)**.

7. With regard to claim 15, Robinett et al discloses a re-multiplexer module **(Figs. 1 and 2, remultiplexers 30 and 100; col. 13, lines 39-41)** comprising:

an input processing portion **(Fig. 2, interpreted as the combination of data link control 112 and direct memory access (DMA) control 116 within each one of several interfaces 110; col. 14, lines 23-32)** that receives a plurality of input data streams **(Fig. 2, TS1, TS2, and TS3; col. 12, lines 58-59)** containing data packets **(col. 6, lines 8-14)**, the input processing portion having a plurality of input interfaces **(Fig. 2, each adapter 110 receives one input stream and**

it is necessarily inherent that the TS would be input through an interface in order to reach data link controller 112 and DMA controller 116), a plurality of input processors **(Fig. 2, interpreted as the combination of data link control 112 and direct memory access (DMA) control 116 within each one of several interfaces 110; col. 14, lines 23-32)**, and a plurality of packet identifier tables **(Fig. 2, cache 114 stores a filter map downloaded and modified by processor 160, col. 14, lines 56-58; *see also* col. 15, line 61 to col. 16, line 2)**, each input interface and packet identifier table corresponding with one of said plurality of input streams **(Fig. 2, each adapter 110 receives one input stream and it is necessarily inherent that the one TS input through the interface in order to reach data link controller 112 and DMA controller 116 and that each adapter 110 uses its own filter map, col. 14, lines 23-32, col. 14, lines 56-58; *see also* col. 15, line 61 to col. 16, line 2)**;

a plurality of packet buffers for storing data packets of said input streams, each packet buffer receiving an input from one of said plurality of input processors **(Fig. 2, each one of multiple adapters 110 (col. 13, lines 55-56) contains a transport packet cache 114 for storing transport packets from one TS (col. 14, lines 47-54) which is then mapped to a corresponding memory location 122 within host memory 120 by DMA controller 116, col. 18, lines 45-67)**;

an output processing portion **(Fig. 2, interpreted as the combination of data link control 112 and direct memory access (DMA) control 116 within each one of several interfaces 110; col. 14, lines 23-32)** that selectively multiplexes data packets **(col. 6, lines 8-14)** from said plurality of buffers **(col. 12, line 58 to col. 13, line 7)** to generate at least two output data streams **(Fig. 2, transport streams (TSs) TS4 and TS5; col. 12, lines 59-62)**, the output

processing portion having at least two output interfaces that act as an output interface to other modules in the MPS **(Fig. 2, each adapter 110 receives one output stream and it is necessarily inherent that each TS would be output through one interface in order to reach its intended audience)**; and

a host processor that controls the operation of the input processing portion and the output processing portion **(Fig. 2, controller 160; col. 13, lines 59-65; *see also* col. 10, lines 45-59)**.

8. With regard to claims 3, 6, 16 and 17, Robinett et al. discloses that the input processing portion includes a plurality of packet identifier tables, each packet identifier table coupled to one of said input processors **(cache 114 stores a filter map downloaded and modified by processor 160, col. 14, lines 56-58; *see also* col. 15, line 61 to col. 16, line 2)**.

9. With regard to claims 4, 5 7, 18, and 19, Robinett et al. discloses that the packet buffer includes an input packet buffer that holds data from accepted packets in the input stream **(Fig. 2, cache 114 for input TSs)** and an insert packet buffer that holds packet data that is to be inserted into the output stream. **(Fig. 2, cache 114 for output TSs)**. Robinett et al. discloses using a filter map (i.e., a routing table) within cache 114 that can be modified **(col. 14, lines 56-58)**. Specifically, Robinett et al. discloses a table of pointers or addresses which processor 160 uses for each specific adapter 110 and maps according to user specification **(Fig. 3, table 402, col. 19, lines 37-60)**. Using a 'current' routing table and updating an 'update' routing table is well-known in the current art to include the use of multiple tables for devices such as switches, routers, bridges, and brouters. Robinett et al. discloses using multiple tables and updating those

tables when necessary **(col. 9, line 63 to col. 20 line 19)** while operating from the active table and switching between the tables to execute correctly ***(see Id.)***. Robinette et al. also discloses combining the information from the multiple input streams (TS1 and TS2) and combining the pertinent portions for an output stream (TS3) by mapping the correct packets from the input queues to the output queues **(col. 2, lines 14-17; col. 23, lines 1-10)**. More importantly, Robinett et al. discloses the use of table 404 for inserting the proper packets in the proper order into the output queue (cache 114) for the output TS **(col. 23, lines 31-43) (*see generally*, col. 18, line 12 to col. 24, line 44)**.

10. With regard to claims 8, 11, 20, and 23 Robinett et al. discloses that the output processing portion includes an output processor **(Fig. 2, interpreted as the combination of data link control 112 and direct memory access (DMA) control 116 within interface 110; col. 14, lines 23-32)** having a bus control logic block that controls the manner in which packets are read from the plurality of packet buffers **(Fig. 2, PCI Bus 130; col. 13, lines 56-58)** as well as links output processing portion, through a system interface, with other modules in a packet processing system **(Fig. 2, controllers 112 and 116 are linked to processor 160, memory 120, and Ethernet/T-1 interfaces 140 and 150, respectively, via bus 130)**.

11. With regard to claims 9-10 and 21-22, Robinett et al. discloses that the output processing portion further comprises a control message processor (message extraction portion) **(Fig. 2, Encryptor/Decryptor 115; *see also* control word information for scrambling/de-scrambling encrypted data in a TS, col. 21, lines 46-63)** that extracts selected messages from the data

stream and stores the extracted messages in any of the plurality of the packet buffers (extracted message buffer) **(Fig. 2, Encryptor/Decryptor 115 periodically examines cache 114 for control words based on the flag set by controller 112 in status bit 129-7, col. 35, lines 1-10; the Encryptor/Decryptor 115 modifies the packets and then re-stores them in cache 114, col. 35, lines 7-10, col. 57-61; *see generally* col. 35, lines 35, lines 7-65)**.

12. With regard to claims 13-14 and 24-25, Robinett et al. discloses that the interface includes at least one output interface to other modules in a packet processing system **(Fig. 2, controllers 112 and 116 are linked to processor 160, memory 120, and Ethernet/T-1 interfaces 140 and 150, respectively, via bus 130)** and an output interface/external equipment interface for each output data stream for devices outside of the packet processing system **(Fig. 2, each adapter 110 receives one output stream via bus 130 and it is necessarily inherent that the TS would be output through an interface in order to reach its intended audience)**.

Conclusion

13. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

(a) De Haas (USP 6,408,436) Bandwidth Optimization of Video Program Bearing Transport Streams. This reference discloses, in Fig. 5, input processing, packet buffers, output processing, at least two outputs, and a host processor.

(b) Lawrence (USP 5,909,468) Method and apparatus for encoding PCR data on a frequency reference carrier. This reference discloses, in Figs. 2 and 5, input processing, packet buffers, output processing, at least two outputs, and a host processor.

(c) Magee et al. (USP 6,02,687) MPEG Transport Stream Multiplexer. This reference discloses, in Fig. 5, input processing, inherent packet buffers, output processing, at least two outputs, and a host processor.

(d) Romanowski et al. (USP 6,233,238) Method for updating clock references in a digital data stream and a remultiplexer. This reference discloses input processing, (inherent) packet buffers, output processing, at least two outputs, and a host processor.

14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mark A Mais whose telephone number is (703) 305-6959. The examiner can normally be reached on 8:00-4:30.

15. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wellington Chin can be reached on (703) 305-4366. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

16. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

August 5, 2004

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